

**AMENDMENTS TO THE CLAIMS**

**This listing of claims will replace all prior versions and listings of claims in the application:**

**LISTING OF CLAIMS:**

1.-11. (canceled).

12. (currently amended): ~~A mobile communication terminal device as set forth in claim 11,~~ A mobile communication terminal device of CDMA system comprising:

a transmission circuit comprising a first code generating circuit for generating a multi-bit code necessary for transmission, a first storing device for storing value of each bit of said first code generating circuit, and a first control device for writing value of each bit at an arbitrary first write timing of said first code generating circuit, and reading the value of each bit stored in said first storage device at an arbitrary first read timing to set to each corresponding bit of said first code generating circuit; and

a reception circuit comprising a second code generating circuit for generating a multi-bit code necessary for reception, a second storing device for storing value of each bit of said code generating circuit, and a second control device for writing value of each bit at an arbitrary second write timing of said second code generating circuit, and reading the value of each bit stored in said second storage device at an arbitrary second read timing to set setting to each corresponding bit of said second code generating circuit.

wherein said arbitrary first write timing, said arbitrary first read timing, said arbitrary second write timing and said arbitrary second read timing are based on discontinuous transmission within a code period,

wherein said first and second code generating circuits are the same circuit that is common to said transmission circuit and said reception circuit.

13. (previously presented): A mobile communication terminal device of CDMA system comprising:

a transmission circuit comprising a first code generating circuit for generating a multi-bit code necessary for transmission, a first storing device for storing value of each bit of said first code generating circuit, and a first control device for writing value of each bit at an arbitrary timing of said first code generating circuit, and reading the value of each bit stored in said first storage device at an arbitrary timing to set to each corresponding bit of said first code generating circuit;

a reception circuit comprising a second code generating circuit for generating a multi-bit code necessary for reception, a second storing device for storing value of each bit of said code generating circuit, and a second control device for writing value of each bit at an arbitrary timing of said second code generating circuit, and reading the value of each bit stored in said second

storage device at an arbitrary timing to set setting to each corresponding bit of said second code generating circuit;

a common shift register portion constituted of shift register having smaller bit number among registers forming respective code generating circuit of said transmission circuit and reception circuit;

a remaining shift register portion constituted of remaining shift register having greater bit number among registers forming respective code generating circuit of said transmission circuit and reception circuit;

exclusive OR circuit and shift register tap for transmission and reception for generating respective of said code necessary for transmission and reception;

switching circuit for switching respective outputs of said exclusive OR circuit, an output of said common shift register portion and an output of remaining shift register portion depending upon transmission and reception,

wherein said first and second code generating circuits are the same circuit that is common to said transmission circuit and said reception circuit.

14. (previously presented): A mobile communication terminal device in a CDMA system designed for interrupting transmitting operation in a discontinuous reception unit period

in a discontinuous transmission, and for interrupting receiving operation in discontinuous transmission unit period, comprising:

a common shift register portion constituted of shift register having smaller bit number among registers forming respective code generating circuit of a transmission circuit and reception circuit;

a remaining shift register portion constituted of remaining shift register having greater bit number among registers forming respective code generating circuit of said transmission circuit and reception circuit;

exclusive OR circuit and shift register tap for transmission and reception for generating respective of said code necessary for transmission and reception;

switching circuit for switching respective outputs of said exclusive OR circuit, an output of said common shift register portion and an output of remaining shift register portion depending upon transmission and reception.

15.-33. (canceled).